FROM POWER PACKAGES TO 3D INTEGRATION : THE THERMAL CHALLENGE

Journée Thématique :

Caractérisations Thermo-physiques et applications micro-électroniques

Christophe SERRE

Innovation Drivers and Consequences

+Functionnality: camera,radio,TV,GPS ,games,internet.==>*integration*

+Mobility: reduced form factor,weight… ==>*miniaturization*

+Performance: pixels,speed,reliability ,less energy greedy..==> *techno. breakthroughs*

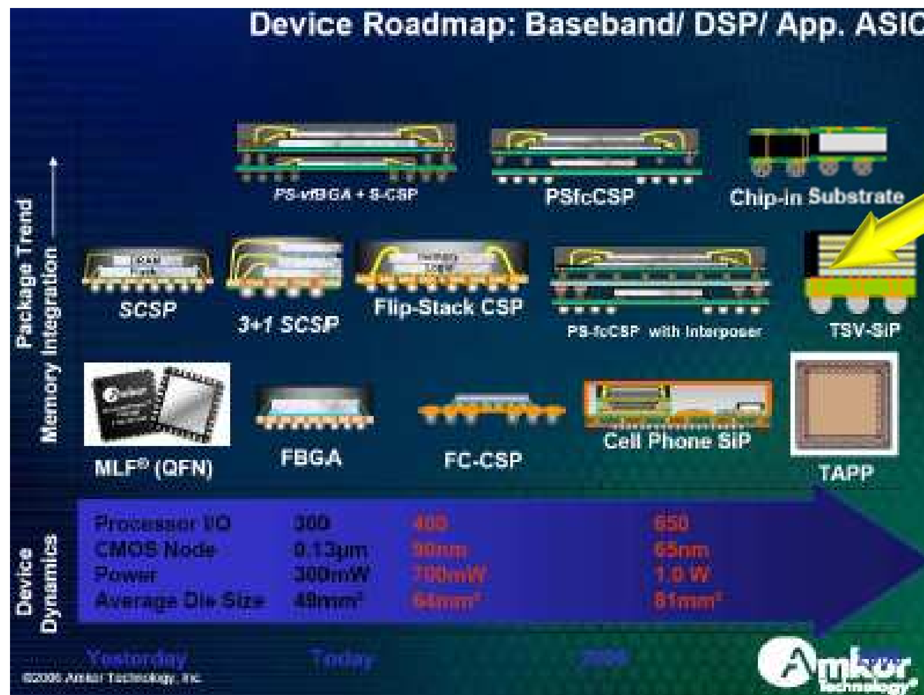
-Price: more for less ==>*cost reduction*

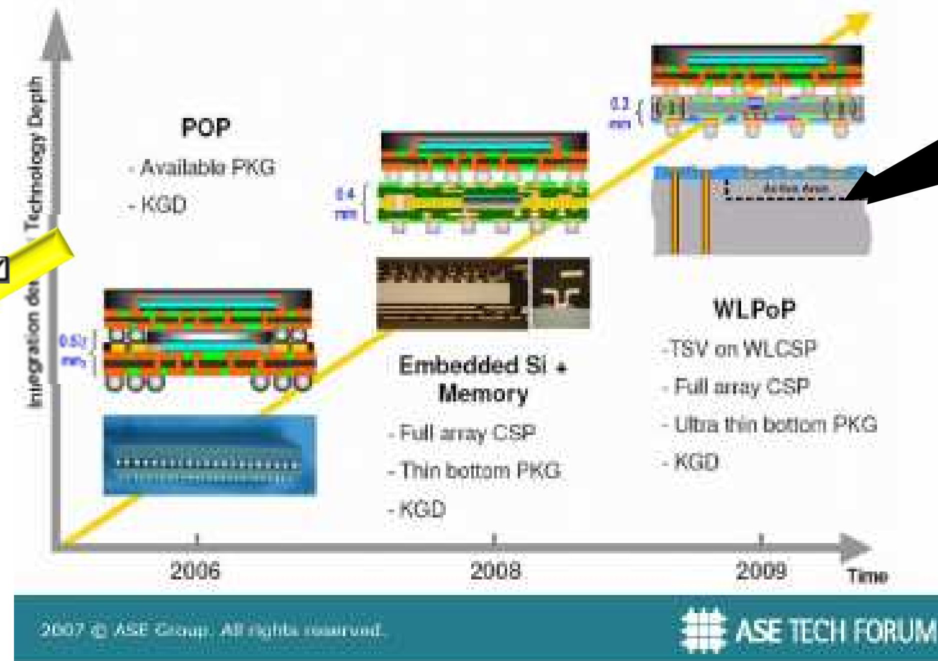
Weigth 3X less
Volume 5X less

3D PACKAGING ROADMAPS

ASE

AMKOR





POWER PACKAGING CHANGES

Surface Mounting

Smaller

Mount Area & Thickness Reduced

Miniaturized

Further Miniaturized

- Low on-Resistance
- High Density Mounting

Thinner

Low Resistance

Low Thermal Resistance

Enhanced Functions (Combined)

KEY AXES OF POWER PACKAGING DEVELOPMENT

INTEGRATION

-Connections: Clips, Ribbon
-Frame evolution
-Dual side Cooling
-Ultra thin dice
-Advanced materials
-..

-Multi Island Packages
-Intelligent Power Modules
-Hi End Power Modules
-Hi Speed Packaging

POWER

-Green molding compound
-Leadfree solder die attach ..

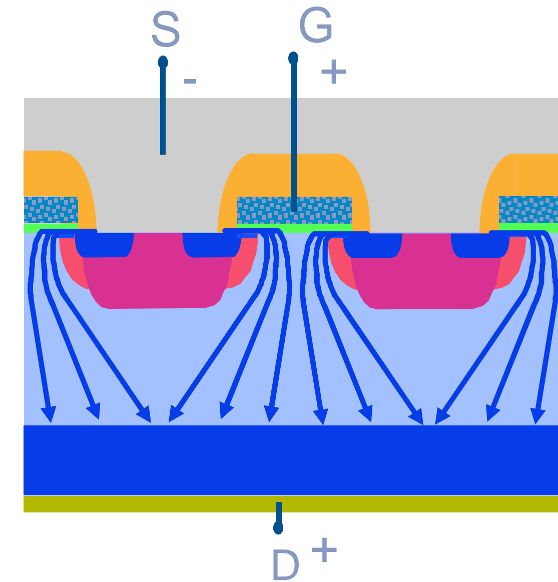
DENSITY

ENVIRONMENT

HEAT EFFECT : THE CHALLENGE!

- Electric Power → Pe = Ron * I^2
- Dissipated Power → Pd= (Tj – Tc) / Rthj

Pd = Pe → Minimum Ron, Minimum Rth



PMOS example

Key Factors for Power Packaging Efficiency

- Interconnections
- Die Attach
- Materials

HEAT DISSIPATION MODES

- **NATURAL WAYS**
  - **Conduction :** heat transfer mechanism due to thermal excitation at molecular level, by direct contact. No motion of material is associated to this mechanism
  - **Radiation :** transport of electromagnetic energy
  - **Natural convection :** transfer of heat associated with the movement of material in a fluid (liquid or gas).
- **FORCED WAYS**
  - Forced convection
  - Components able to absorb heat with power (Pelletier effect, refrigerating machines)
  - Use of some materials ‘s latent heat of phase change (caloducs, thermo-siphons, fluids evaporation, etc…)

HEAT DISSIPATION MODES

Convection & Radiation

Conduction

Conduction

Conduction

Convection & Radiation

MATERIALS THERMAL CONDUCTIVITY

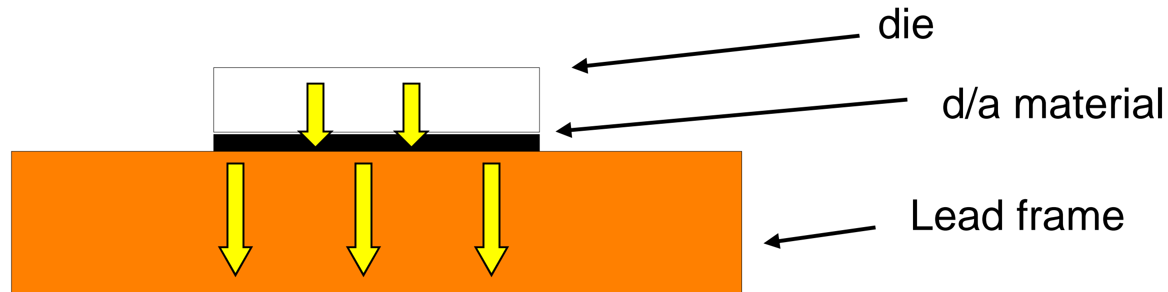
- **Silicium** $\frac{1}{\sigma} = 3.14 * 10^{-3} * T^{-0.219}$ ie 140W/mK@25°C, 113W/mK@100°C & 88W/mK@150°C
- **Glass** = 1.2 W/m.k
- **Sapphire** = 42 W/m.k

- **Copper** = 260 to 400 W/m.K
  - Alloy 194 = 260
  - KFC, FPG = 360
  - Cub2 = 370
  - Cua1= 390
  - Alloy42 (FeNi) = 40
- **D/A materials**
  - PbSnAg = 30 to 45

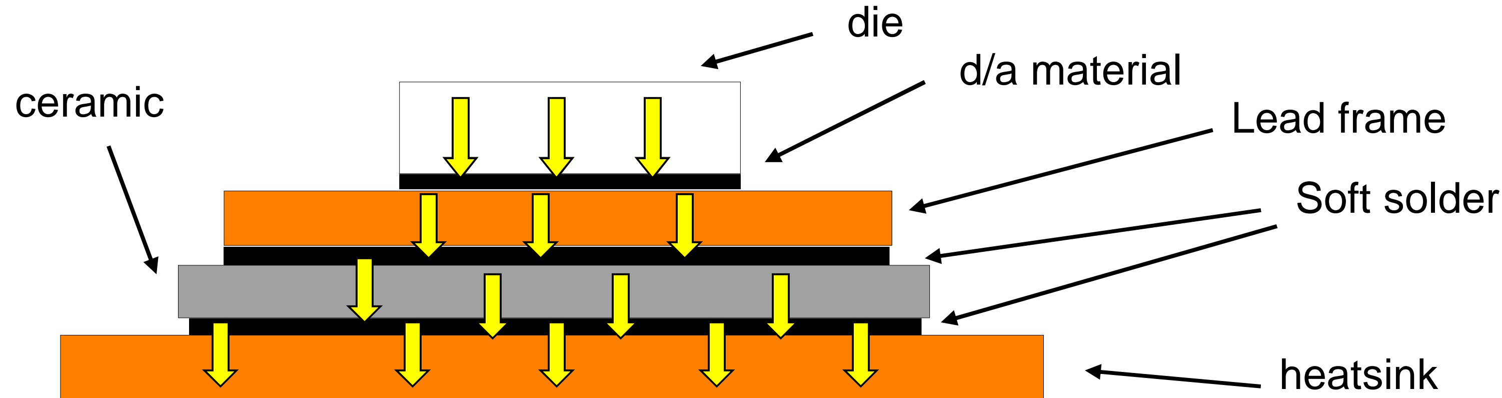
    PbSn5Ag1.5 = 42, PbSn5Ag2.5=44, SnPb37=70
  - Silver glue = 2 to 6
- **Resins**
  - Standard EMC (fused silica) = 1
  - Conductive EMC (crystallized silica) = 2.5
- **Ceramics**
  - Al2O3 = 20 to 25
  - AlN =170-180
- **Wires**
  - Al = 200

MULTIPLE INTERFACES EFFECT ON Rth

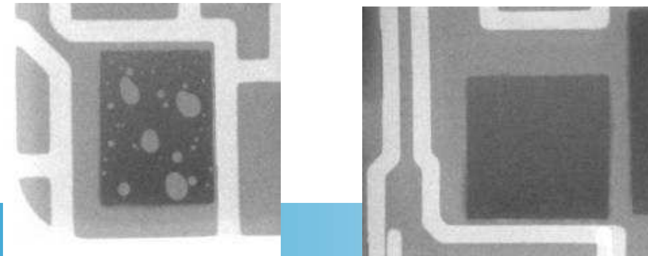
NON INSULATED PACKAGES (TO220, TO247, DPAK,…)



CERAMIC INSULATED PACKAGES (TO220I, TOP3, RD91,…)



SOLDER JOIN QUALITY



DIE THICKNESS REDUCTION

- To improve the thermal performance of our devices by reducing the silicon thickness
- Special F/E-B/E manufacturing process to solve the warpage and the handling problem that occurs when we reduce the wafer thickness down to 100µm or below

COPPER LEAD-FRAME DESIGN EFFECT ON Rth

Rth (package)

4
3.5
3
2.5
2
1.5

1.27 mm slug version 1
1.27 mm slug version 2
0.5 mm slug version 3

0 5 10 15 20 25

Ssi (mm^2)

version 1

version 2

version 3

PACKAGE SIZE EFFECT ON Rth

Rth (°C/W)

2.5
2
1.5
1
0.5
0

Theoritical Guaranteed

SOT 32
I-Pak
SOT 82
MAX 220
TO 220 family
TO 247
MAX 247

0 20 40 60 80 100 120

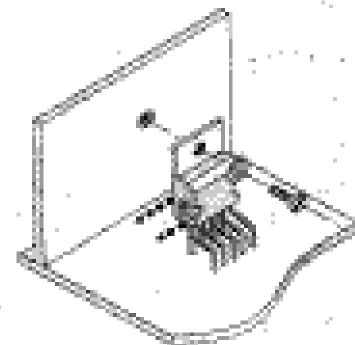
Ssi (mm²)

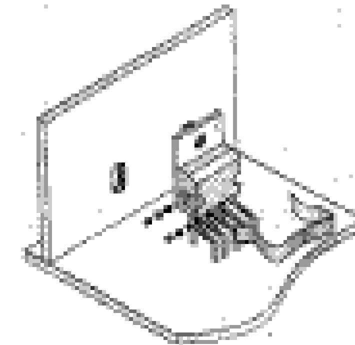
with die thickness of 300 µm, periphery of 200 µm & σ(Si) of 110 W/mK

EXTERNAL HEATSINK INFLUENCE

- **Non insulated Insertion packages (TO220, TO247,…)**
  - Inserted in through hole technology boards
  - Secured to external heatsink using screws or clip (cheaper)
- **Insulated insertion packages (ISOWATT220, ISO218, ..)**
  - When insulation is mandatory, thin sheet of mica or adhesive mylar can be placed between slug and heatsink

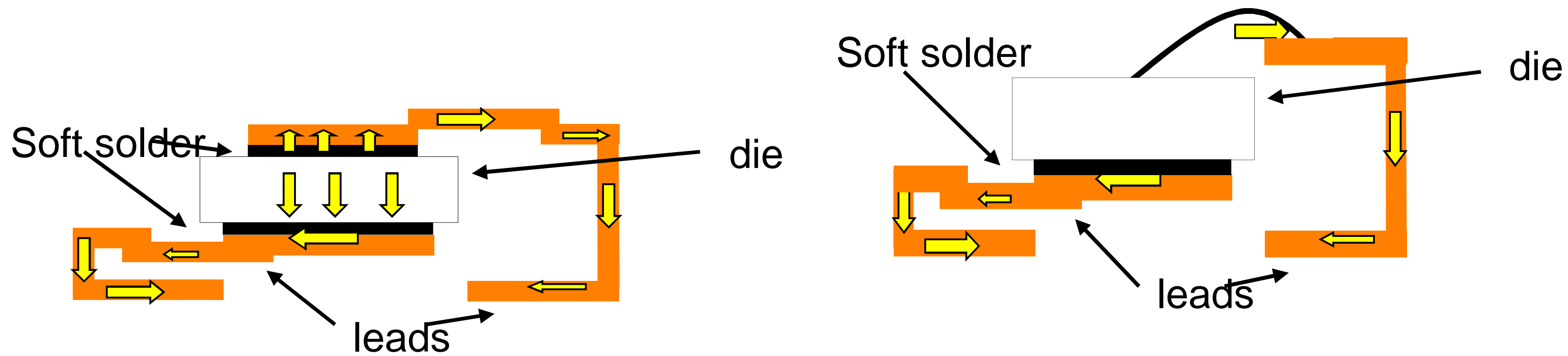
Problem : thermal performance inconsistent (variations in thickness, position and adhesion of the insulating sheet)

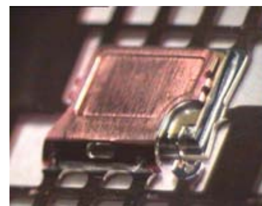


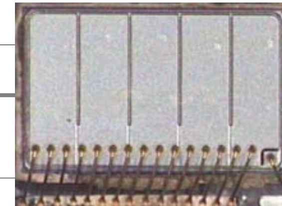


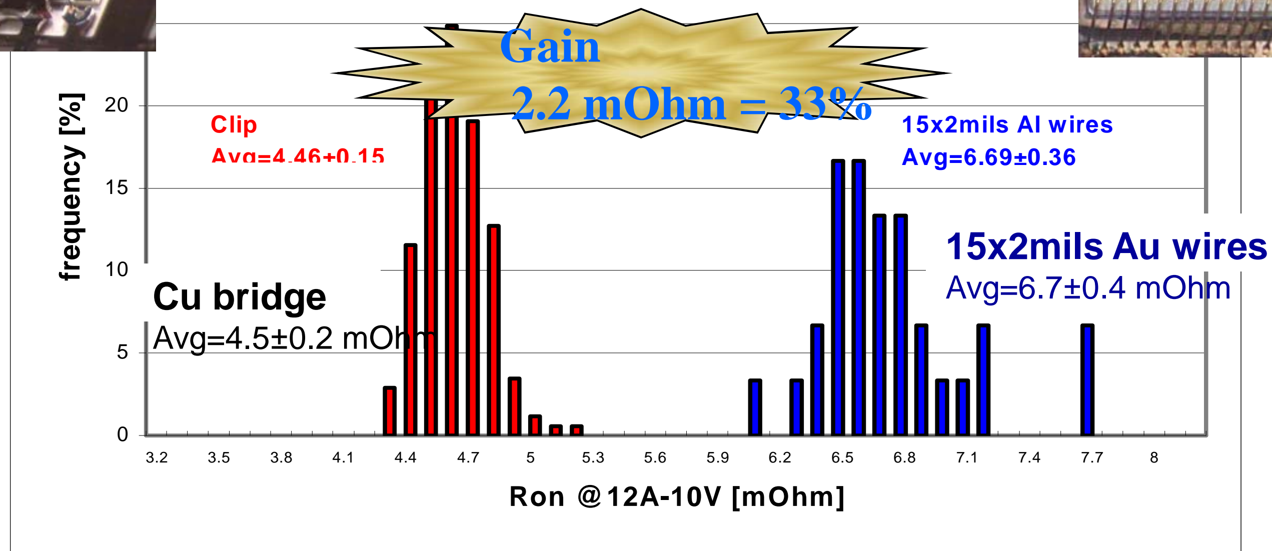
PACKAGE	ISOLATION	Rthj-c °C/W
TO-220	none	1.3
TO-220	100mm mica	3.3
TO-220	mylar	4.4
ISOWATT220	none	3.0
ISOWATT221	none	3.8
ISOWATT218	none	2.1

DIE TOP INTERCONNECTION EFFECT ON Rth

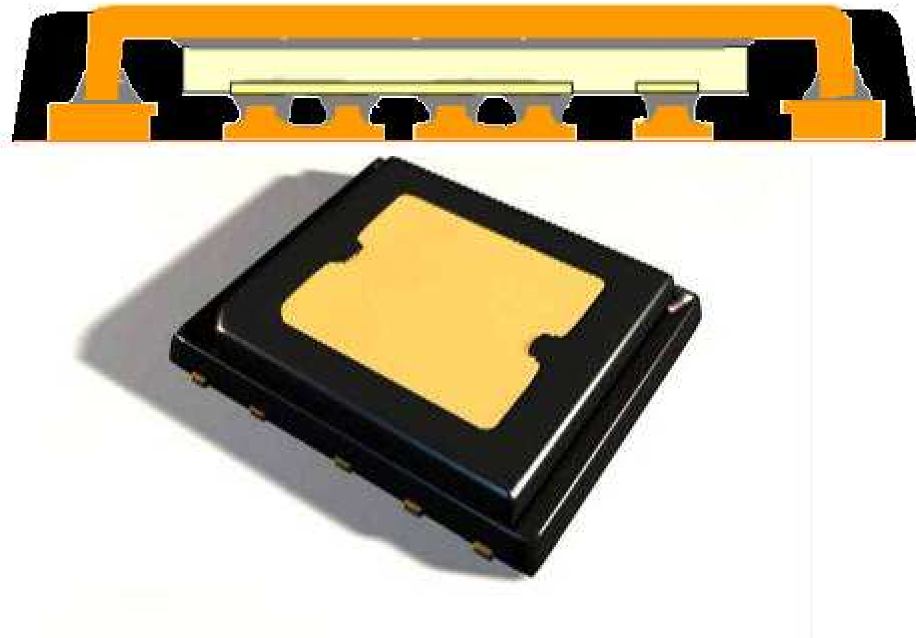


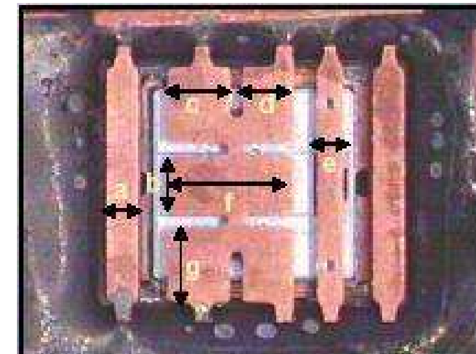


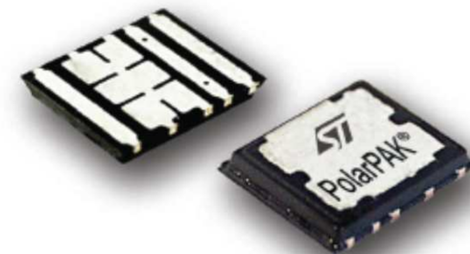




DUAL SIDE COOLING

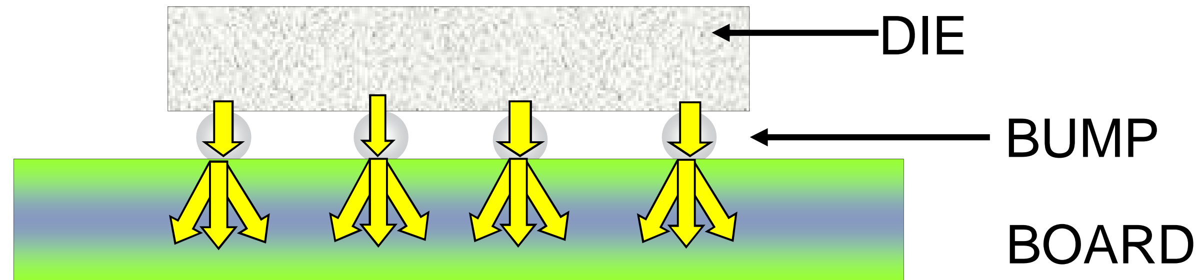


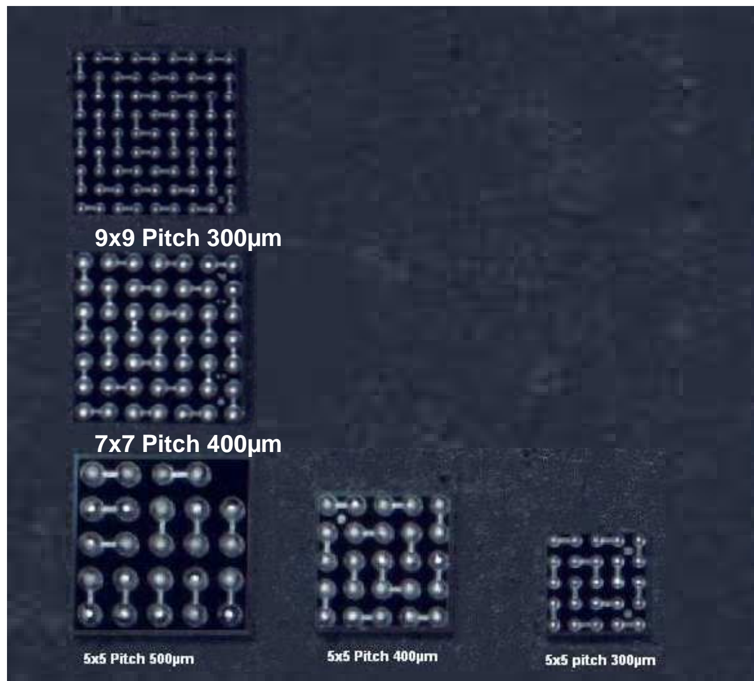


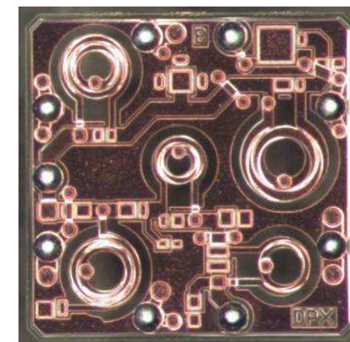


Rth improvement: Dissipation by Top

WAFER LEVEL SIMILARITIES







DIE SIZE / IO NUMBER EFFECT ON Rth

Epoxy FR4, e_{CU}=35µm

$R_{th(j-a)}$(℃/W) vs S(mm²)

- Y axis: 50, 100, 150, 200, 250, 300, 350
- X axis: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10
- Labels: 6 bumps, 8 bumps, 16 bumps, 24 bumps
- Board ESDALC6V1F1

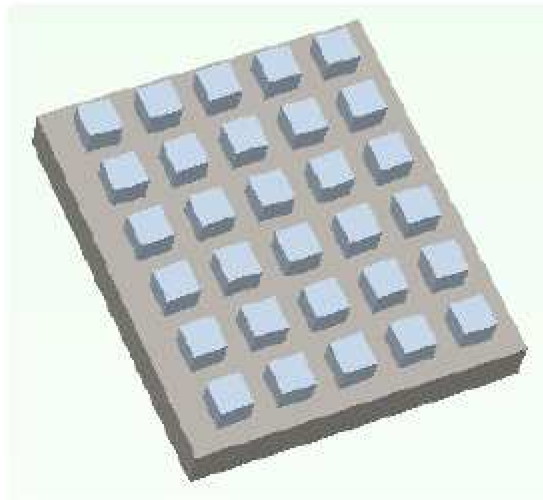
Thermal resistance junction to ambient versus die surface (typical values)

PRINTED WIRING BOARD EFFECT ON Rth

	D-Pak Rth (j-a)	D^2-Pak Rth (j-a)
On infinite heatsink	2.5 °C/W	1 °C/W
FR4	65 °C/W	50 °C/W
FR4 with 10 cm^2 on board heatspreader	40 °C/W	35 °C/W
FR4 with copper filled holes on heatsink	13.5 °C/W	12 °C/W
IMS floating in air	9.5 °C/W	8 °C/W
IMS with external heatsink	4.5 °C/W	3 °C/W

assuming a heatsink of 2 °C/W

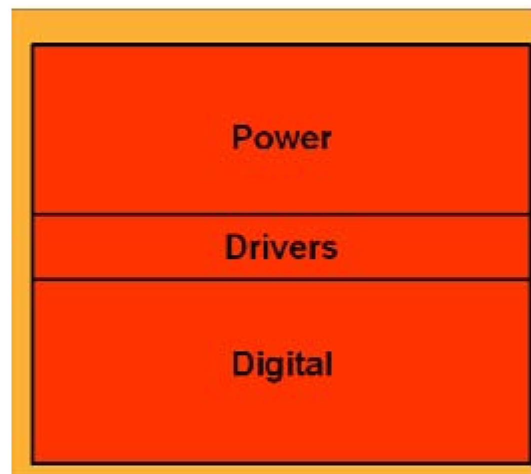
CASE STUDY : DESIGN PARAMETERS EFFECT ON Rth


Package bottom view

WCSP 3.1x2.7x0.65 mm

30 balls / Lead free
(5x6 matrix)
0.3 mm diameter
0.5 mm pitch

die size = 3.102 x 2.738 mm
die thickness = 400 µm



Source	Area (mm^2)	Power (mW)
Power	2.85	760
Drivers	1.02	665
Digital	3.09	165

Total Area = 6.97 mm^2

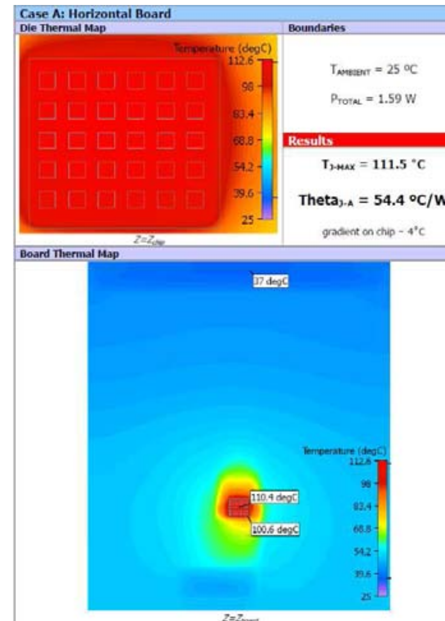
Total Power = 1.59 W

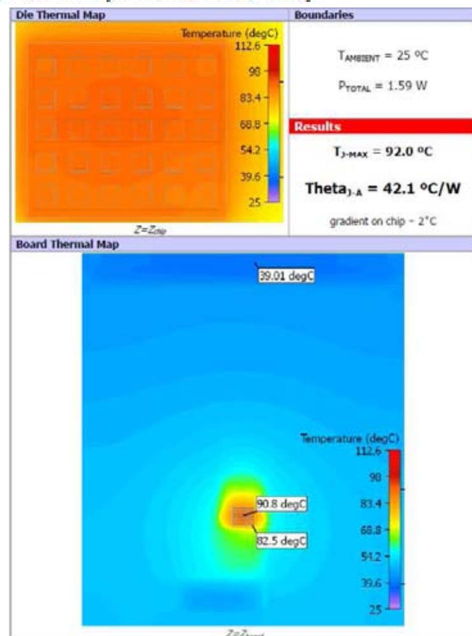
THE CONDUCTION EFFECT IS KEY

Steady State Conditions

Different cases have been evaluated:

- **CASE A:** Horizontal board
- **CASE B:** Vertical board
- **CASE C:** Bar instead of balls
- **CASE D:** Die thickness 200 µm instead 400 µm
- **CASE E:** Layer thickness 2 oz. instead 1 oz.
- **CASE F:** Underfill (k = 0.4 W/mK)





Case	Difference to Case A
Case A (Horizontal Board)	---
Case B (Vertical Board)	-2.9 %
Case C (Bar)	+0.5 %
Case D (Die Tck 200 µm)	+1.3 %
Case E (Layer Tck 2 oz.)	-22.5 %
Case F (Underfill)	-0.4 %

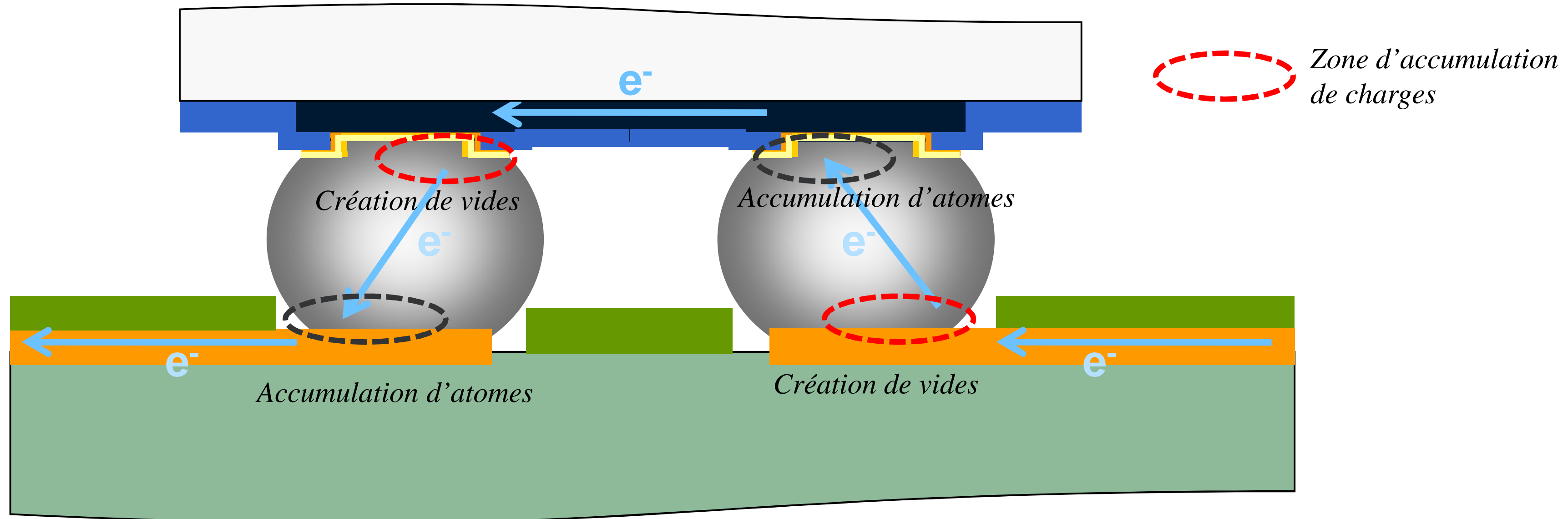
OTHER THERMAL EFFECTS

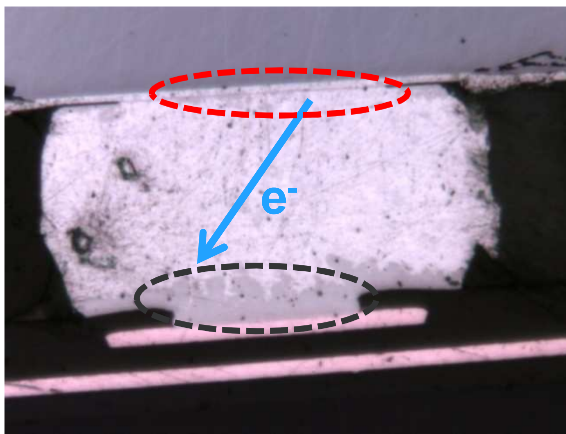
- Electro migration
  - Black's law

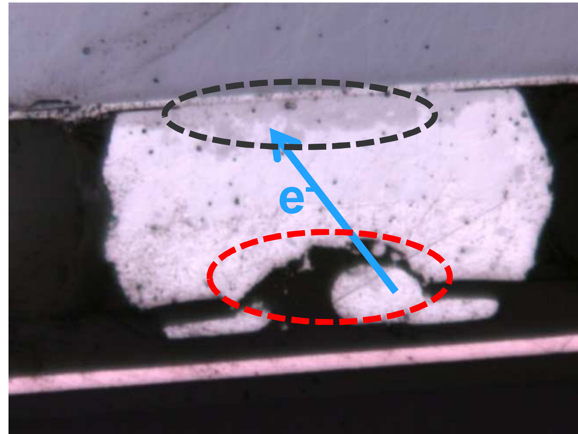
$$TTF = A \cdot J^{-N} \cdot \exp\left(\frac{E_a}{k \cdot T}\right)$$

  - Key factors :
    - Current Density J
    - Temperature T
  - Main failure mode :
    - Current crowding in some particular location heats the structure.
    - Voids are created, increasing the current density and the heating of the structure
- Thermo migration
  - The component ambient operating temperature can drastically influence the aging speed. Especially a temperature gradient between the component and the board (from 0.15°C/µm) can damage the bump

ELECTROMIGRATION EFFECT

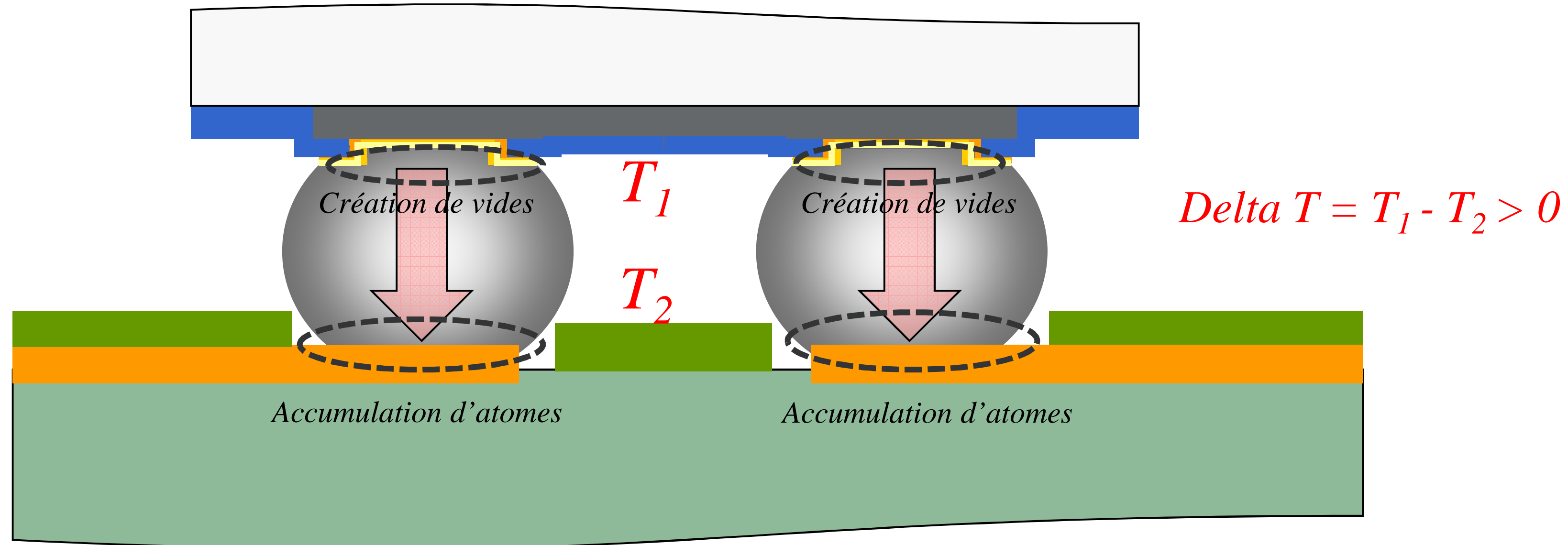




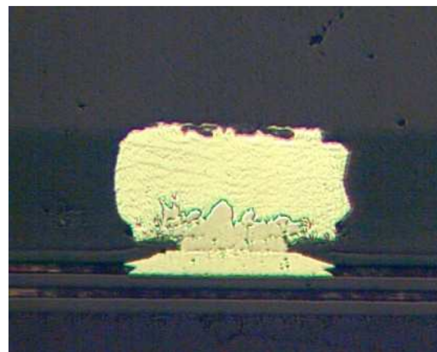


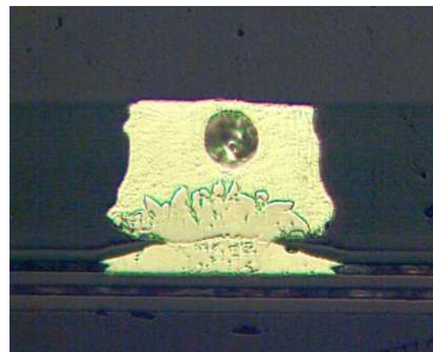
Courant électrique = 400mA
T ambiante =125 °C
Microsection @ 320 hours
Bossage en SnAg4Cu0.5

THERMOMIGRATION EFFECT



Delta $T = T_1 - T_2 > 0$

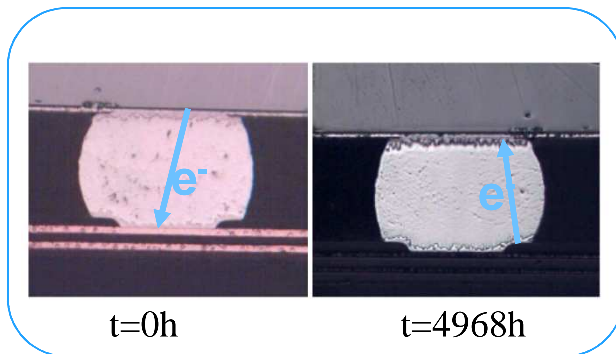




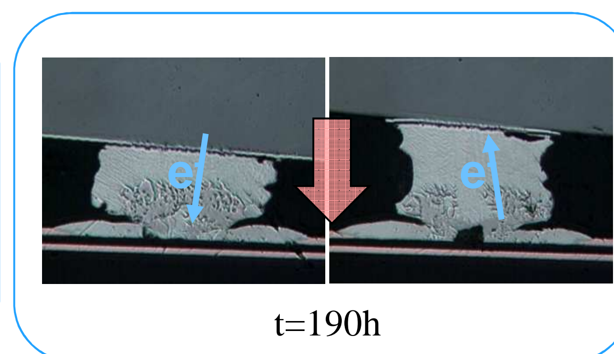
Pas de Courant électrique
Delta T = 0.2 °C/µm
Microsection @ 60 hours
Bossage en SnAg4Cu0.5

COMPONENT DESIGN EFFECT

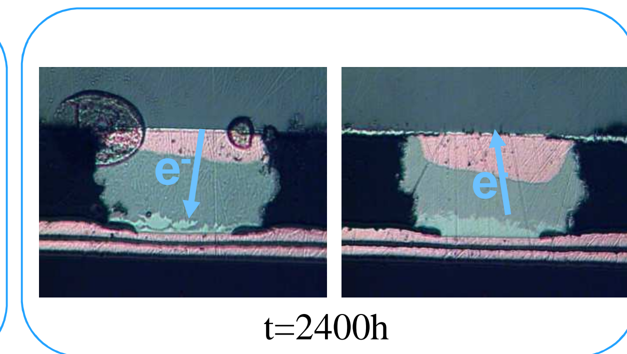
Daisy Chain Component	Active Component	Active Component
⇒ No Heating	⇒ Heating	⇒ Heating
⇒ Solder Bump	⇒ Solder Bump	⇒ Copper Pillar Bump (Low Bump Rth)



t=0h t=4968h



t=190h



t=2400h

Scenario 1

Ta = 25°C
Tj = 30°C
I = 240mA
J = 0.12mA/µm²
Grad T = 0.001°C/µm

No Defect@ 4968h

Scenario 2

Ta = 25°C
Tj = 156°C
I = 240mA
J = 0.12mA/µm²
Grad T = 0.295°C/µm

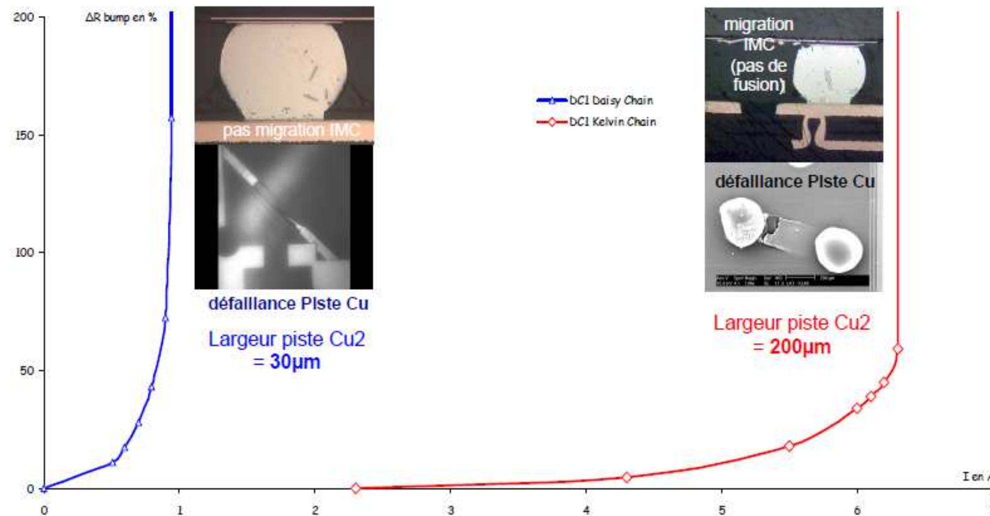
1st Defect @ 180h
$TTF_{63.2\%}$ = 245h

Scenario 3

Ta = 25°C
Tj = 164°C
I = 240mA
J = 0.12mA/µm²
Grad T = 0.114°C/µm

No Defect@ 2400h

FUSE EFFECT

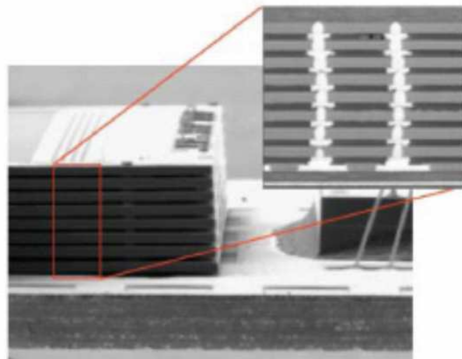


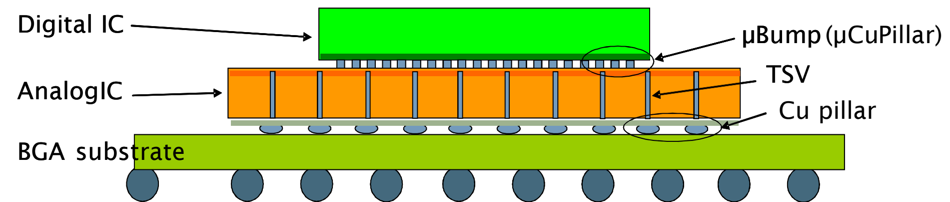
❑Resulting from the Joule effect, either the bump or the component structure can be heated and in certain the extend fuse.

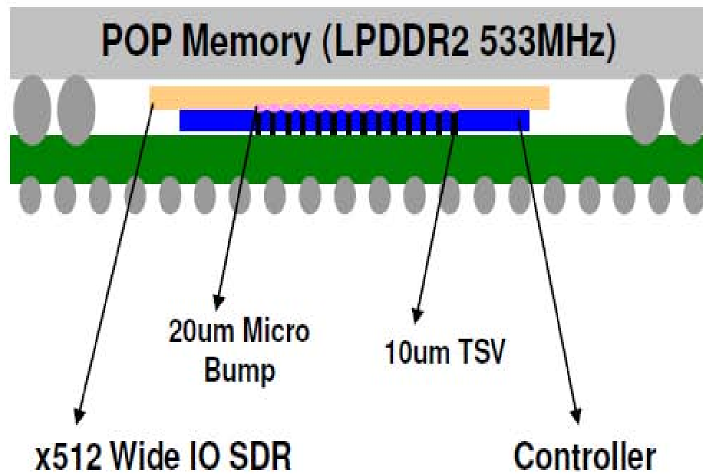
❑Key parameters are :

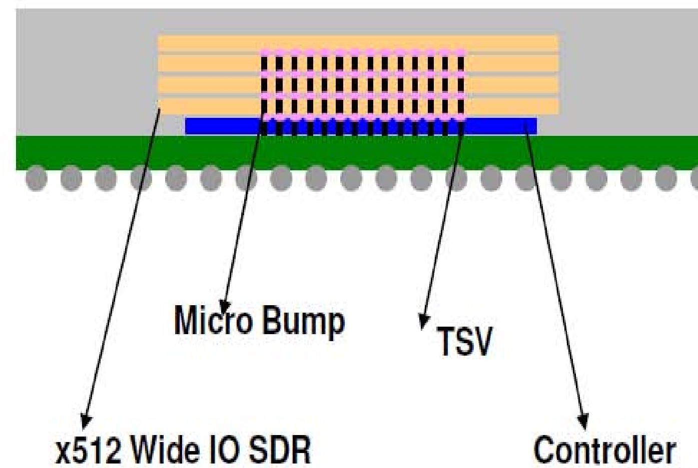
- ❑The bump material
- ❑The bump size
- ❑The component and PWB design (Line width, Line thickness, Thermal vias,…)
- ❑The component and the PWB materials (Glass, Silicon, …)

3D COMPONENT = 3X COMPLEXITY

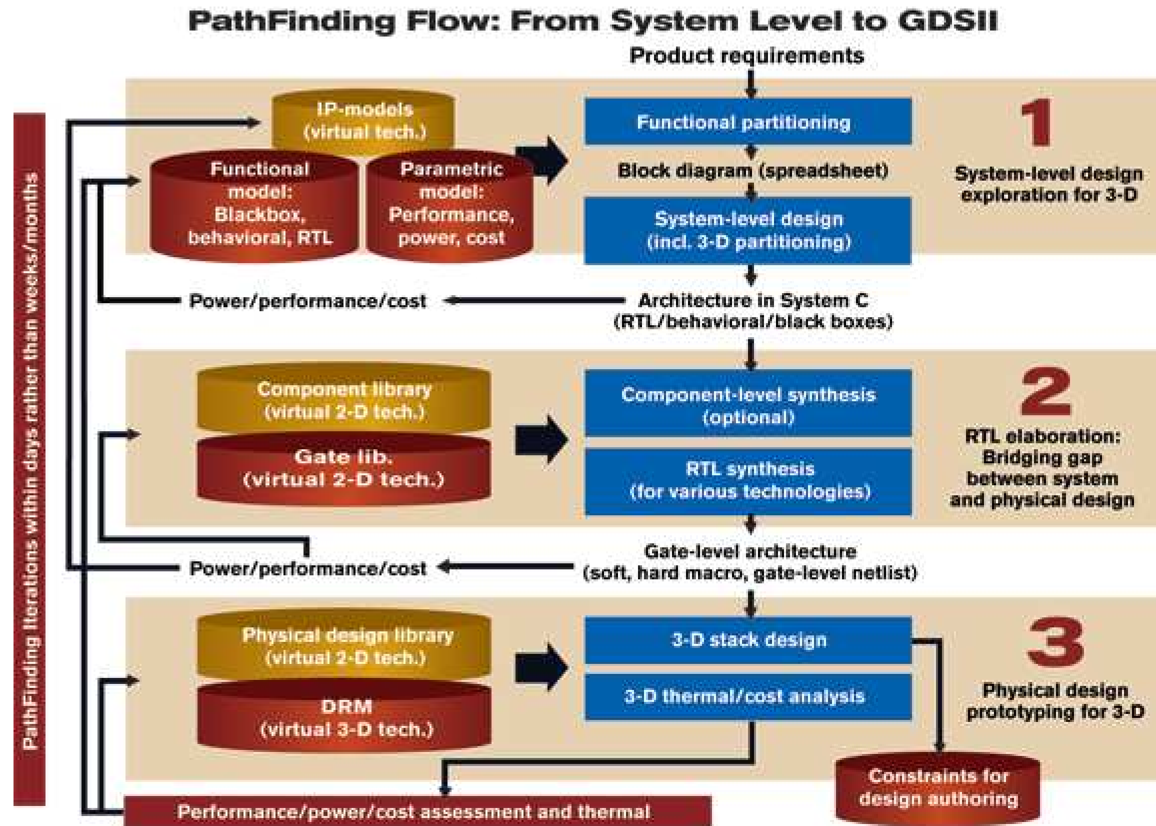








3D DESIGN CHALLENGES:THINK GLOBAL



Main shift in Design paradigm:
3D means to think B-E and F-E at the same time

THANK YOU!